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Side-Channel Security Analysis of Ultra-Low-Power FRAM-based MCUs

14. April 2015

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Story?

- MSP-EXP430FR5969 (kit)
- MSP430FR5969 (MCU)
 - FRAM
 - Ultra-Low Power
 - AES (hardware)





Story? (FRAM)

- non-volatile like flash
- much faster than flash (@ write) "125 ns"
- much less power than flash (@ write) "82 μA/MHz"
- super high write cycles "10¹⁵"
- destructive (each read is followed by a write)
 - read speed limited to write speed
 - currently @ 8MHz
 - small cache for higher speeds (16MHzs)



Story? (Low-Power)

WHITE PAPER

Jacob Borgeson , MSP430 product marketing engineer Texas Instruments

Texas Instruments

Introducing advanced security to low-power applications with FRAM-based MCUs

Introduction

Security is becoming increasingly important in a wide range of applications including smart phone accessories, smart metering, personal health monitoring, remote controls and access systems. According to a recent study conducted and published by ECN, the market for secure applications is expected to grow by 45% CAGR over the next five years¹.

While security of data and operations has always been a consideration for several of these applications, the rising financial risks Consider a mobile credit card payment system that enables a merchant to process credit cards using a dongle connected to a mobile phone. Being able to compromise one of these devices would enable unscrupulous merchants to record confidential customer information for later use in fraudulent transactions. Alternatively, the ability to alter readings from electricity meters would allow consumers and businesses to substantially reduce their utility bills while shifting the costs to utilities and other customers. In fact, one reason why meters are moving from electromechanical systems to semiconductor-based "smart meters" is that the electromechanical portion can be easily tricked with a few magnets.





Story? (Low-Power)

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 Power analysis: Spectral Power Analysis (SPA) and Dynamic Power Analysis (DPA) are specialized techniques where the electromagnetic emissions or power usage of an MCU is measured to create a profile that can be used to determine what the MCU is doing internally. EEPROM and Flash require a charge pump operating at 10 to 14 V, which makes them relatively easy to detect. The extremely fast read and write speed of FRAM (less than 50 ns and 200 ns respectively), as well as its lower operating voltage (1.5 V) make it much more difficult to successfully mount an SPA- or DPA-based attack against.



Story? (AES)

- Supporting 128, 192, 256 key sizes
- Supporting ECB, CBC, OFB, CFB
- Supporting pre-computed and on-the-fly KeySchedule
- not super fast

Key length	Encryption (clock cycles)	Decryption (clock cycles)
128 bits	168	168
192 bits	204	206
256 bits	234	234

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Setup





Setup







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Setup matters?





AES (hardware)

AES-128 encryption (really low power)





AES (software)

- taken from <u>http://www.ti.com/tool/AES-12</u>8
- @ first glance, variable timing -> MixColumns

unsigned char galois_mul2 (unsigned char value)
{ if (value > >7) {
 return ((value << 1) ^ 0 x1b); } else
 return (value << 1) ; }</pre>

- Conditional branch!
 - vulnerable to state-of-the-art timing attack
 - vulnerable to SPA





AES (software) @ 8MHz

Much more power consuming than the hardware module





cache

-64-bit

set 0, line 0

set 0, line 1

set 1, line 0

set 1, line 1

Cache / AES (software) @ 16MHz

- two-way set-associative
- pretty small
- shared
 - both program and data
- opens new doors for SCA
 - trace-driven cache attacks
 - may face many challenges due to its shared fashion

16

FRAM

64-bit

Address: 0

Address : 1

Address : 2

Address: 3

Address: 4

Address : 5

17

SubBytes @ 16MHz



18 Time [μs]

19

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Internal Architecture

- mainly unknown to the end users
- pipelined CPU architecture with ??? stages
- usually such unknown architectures cause masked implementations to be still vulnerable
- Case study: S. Kerckhof, FX. Standaert, and E. Peeters @ CARDIS 2013 "From New Technologies to New Solutions - Exploiting FRAM Memories to Enhance Physical Security"







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- 16-bit state and 4 rounds
- measurements excluding tables' pre-computation





non-specific (fixed vs. random) 1st-order *t*-test







- These two memory locations cleared before being measured
- mov #STATE , pointer
- mov.b #0x00,0(pointer)
- mov.b #0x00,1(pointer)



still 1st-order leakage



- intensive investigations by inserting several nop instructions between probable leaky instructions
- finally, (masked) table look-ups
 - "reading from the tables stored in FRAM"

mov.b @pointer,m0

- several attempts to avoid the leakage
 - e.g., by clearing the target register m0 beforehand
 - no success...



Sum up

- state-of-the-art attacks on unprotected device
 - expected results
- difficulties on measurements due to the low-power design
 - a suitable method to measure
- AES hardware accelerator, attackable but not easily
- software implementations highly vulnerable
- cache may become a leakage source
- unknown internal architecture may turn a masked implementation into a vulnerable design
- This work just gives an overview about the possible leakage sources when such a platform is being used in security-critical applications.



Thanks! any questions?

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