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Trade-offs in protecting Keccak against combined side-channel and fault attacks

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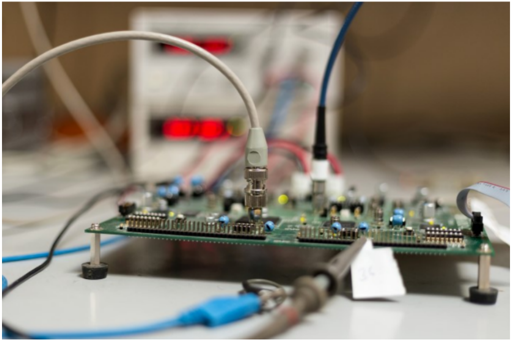
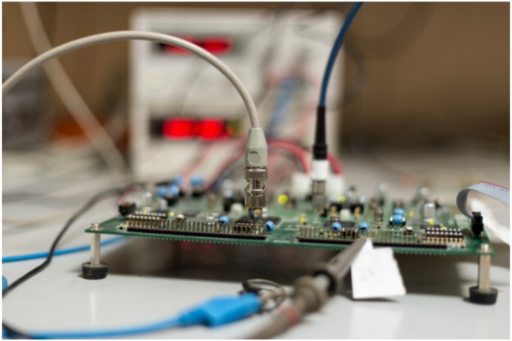
April 5, 2019

Physical attacks



- Side channel analysis
- Fault injection

Physical attacks



- Side channel analysis
- Fault injection
- Combined attacks - combined countermeasures: ParTI [SMG16], M&M [DAN+19], Capa [RDB+18]

Outline

CAPA

Protected implementations of KECCAK

Security evaluation

Conclusion

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Adversarial model: tile-probe-and-fault

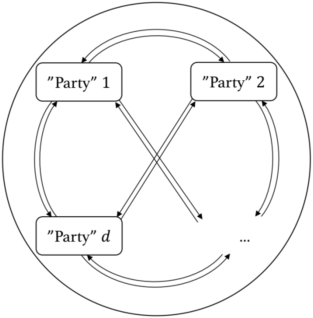

Figure: Tile architecture [RDB+18]

At least one of the d tiles shall remain uncompromised

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Representation

- Finite field $\mathbb{F}_q = GF(2)$
  - Addition is denoted $+$, $\sum$
  - Multiplication is denoted $\cdot$, $\prod$

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  - MAC key is shared between the d tiles s.t. $\alpha = \sum \alpha_i$

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- Representation of a secret value $x \in \mathbb{F}_q$ in the masked domain

$$\langle x \rangle = (\boldsymbol{x}, \boldsymbol{\tau}^x)$$

Data shares $\boldsymbol{x} = (x_1, x_2, \ldots, x_d)$ such that $x = \sum x_i$
Tag shares $\boldsymbol{\tau}^x = (\tau_1^x, \tau_2^x, \ldots, \tau_d^x)$ such that $\tau^x = \sum \tau_i^x$

Computing procedure - addition

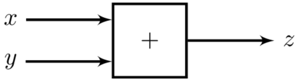


Figure: Original addition

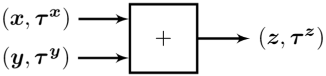
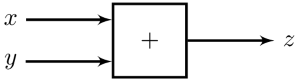


Figure: Masked addition

Computing procedure - addition



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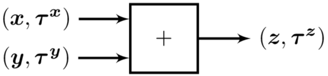

Figure: Masked addition

- Each tile $\mathbb{T}_i$ locally computes its share of the output z
  - Data share $z_i = x_i + y_i$
  - Tag share $\tau_i^z = \tau_i^x + \tau_i^y$

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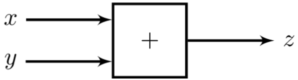

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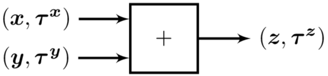

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  - Tag share $\tau_i^z = \tau_i^x + \tau_i^y$
- *Correctness.*

$$\sum z_i = \sum (x_i + y_i) = \sum x_i + \sum y_i = x + y = z$$
$$\sum \tau_i^z = \sum (\tau_i^x + \tau_i^y) = \sum \tau_i^x + \sum \tau_i^y = \tau^x + \tau^y = \tau^z$$

Computing procedure - multiplication

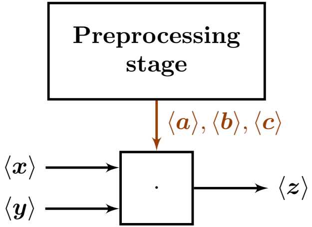

Figure: Auxiliary triple for multiplication

- Using Beaver triple $\langle a \rangle$, $\langle b \rangle$, $\langle c \rangle$ where $c = a \cdot b$
- Two-cycle latency
- MAC tag check

Capa

- Evaluation and preprocessing stage
- Number of tiles $d \Longrightarrow (d-1)$th order SCA resistance
- Security parameter $m \Longrightarrow$ fault detection probability $1-2^{-m}$
  - m independent MAC keys α

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KECCAK-f permutations

- Permutation width $b \in \{25, 50, 100, 200, 400, 800, 1600\}$
- Round function R
- Number of rounds $n_r = 12 + 2\log_2(w)$, where $w = \frac{b}{25}$

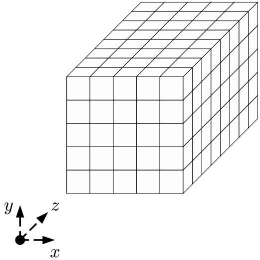

Figure: The KECCAK state [BDPVA09]

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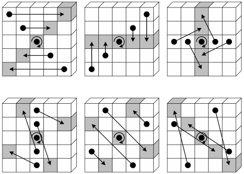
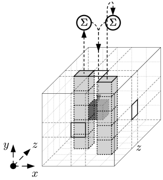
KECCAK-f permutations

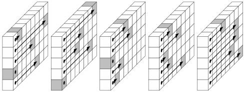
$$R = \iota \circ \chi \circ \pi \circ \rho \circ \theta$$



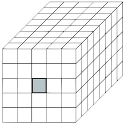
π



θ



ρ



ι

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KECCAK-f permutations

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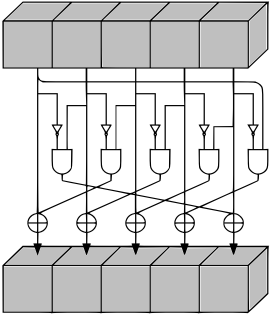

Figure: The χ step mapping [BDPVA09]

- b multiplications each round
- Most expensive operation

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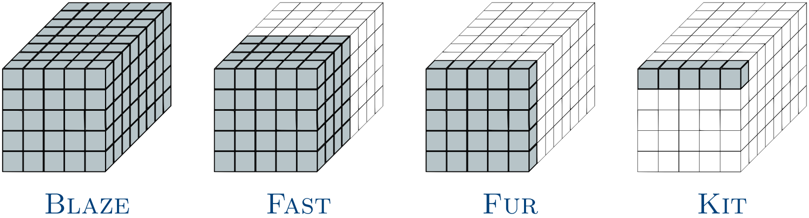
The speed-area tradeoff

$$R = \iota \circ \chi \circ \pi \circ \rho \circ \theta$$



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Blaze - high throughput

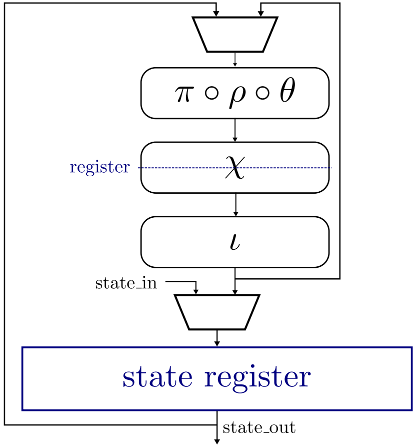
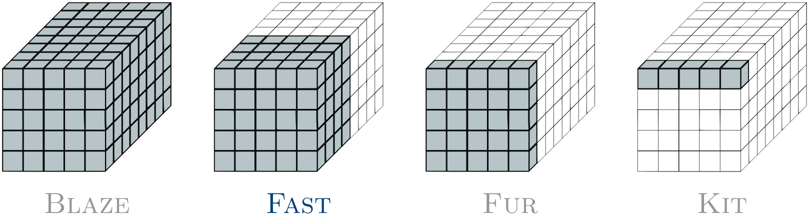


Figure: High-level architecture for Blaze

The speed-area tradeoff

$$R = \iota \circ {\color{red}\chi} \circ \pi \circ \rho \circ \theta$$



FAST - moderate throughput

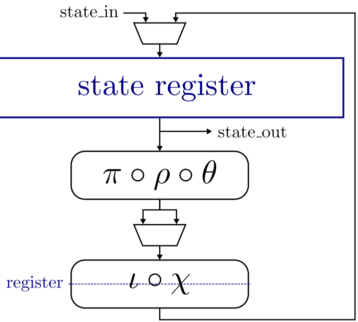
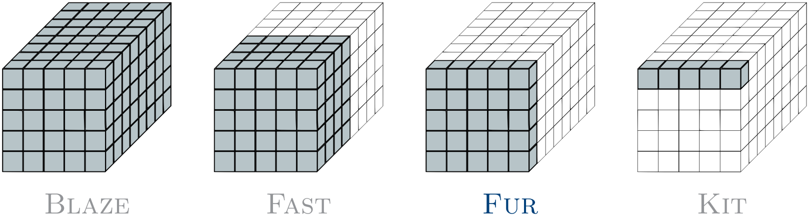


Figure: High-level architecture for FAST

- Half state for $\iota \circ \chi$
- Full state for $\pi \circ \rho \circ \theta$
- ≈ 3 cycles per round

The speed-area tradeoff

$$R = \iota \circ \chi \circ \pi \circ \rho \circ \theta$$



Slice-based processing

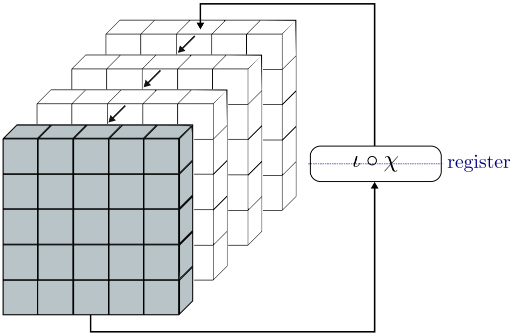


Figure: Slice-based processing

FUR - moderate area

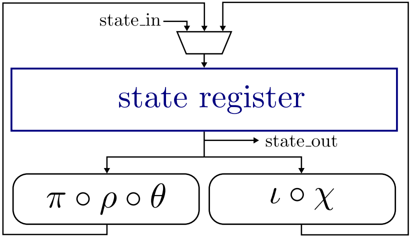
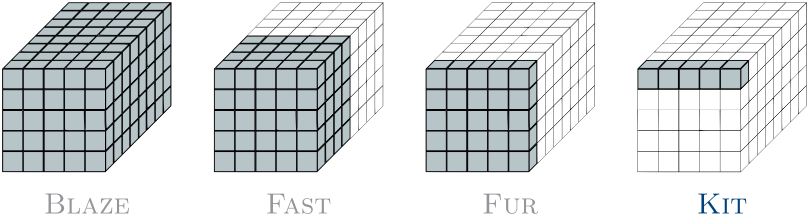


Figure: High-level architecture for FUR

- Full state for $\pi \circ \rho \circ \theta$
- Slice-based for $\iota \circ \chi$
- $\approx w + 2$ cycles per round

The speed-area tradeoff

$$R = \iota \circ \chi \circ \pi \circ \rho \circ \theta$$



Row-based processing

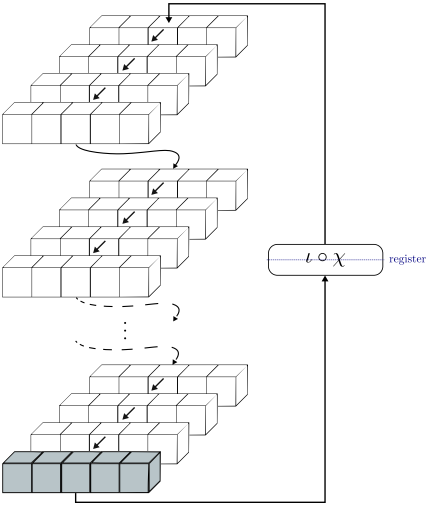


Figure: Row-based processing

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KIT - low area

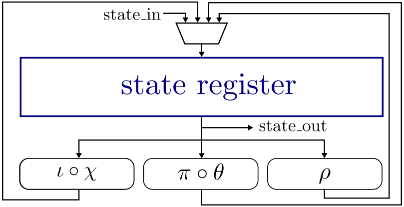
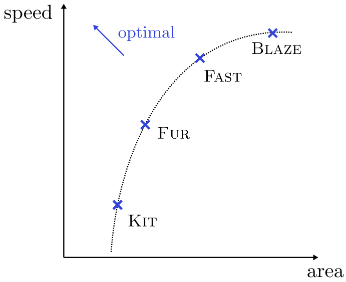


Figure: High-level architecture for KIT

- Slice-based for $\pi \circ \theta$
- Slice-based for ρ
- Row-based for $\iota \circ \chi$
- $\approx 7w + 1$ cycles per round

Summary



Design	S-boxes (χ)	Preprocessing	Cycle count
BLAZE	$b/5$	b	$n_r + 2$
FAST	$b/10$	$b/2$	$3 \cdot n_r + 1$
FUR	5	25	$(w+2) \cdot n_r + 1$
KIT	1	5	$(7w+1) \cdot n_r + 1$

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Outline

Literature comparison

Order	Design	AREA [kGE] Evaluation χ	θ	State	Σ	Prep.	Total	Rand. [bpc]	f_{max} [MHz]	Cycles [/]
KECCAK-f[1600] in NANGATE 45nm ($m=0$)										
1	BLAZE	145.1	12.8	33.7	199.7	231.0	430.7	16000	892	25
	Parallel [GSM17]	38.4	15.0	32.2	85.7	-	85.7	480	891	48
	Parallel-3sh [BDN+13]	40.6	19.2	56.8	116.6	-	116.6	4	592	25
2	BLAZE	235.2	19.2	50.5	317.1	449.3	766.4	28800	884	25
	Parallel [GSM17]	114.0	22.5	51.1	188.1	-	188.1	4800	898	48
KECCAK-f[200] in NANGATE 45nm ($m=0$)										
1	BLAZE	18.1	1.6	4.2	25.2	28.9	54.0	2000	892	19
	5-10-5 [ABP+18]	73.4	14.0	11.9	99.3	-	99.3	-	395.25	9
	6-6-6 [ABP+18]	44.6	11.3	14.2	70.1	-	70.1	-	436.7	9

Table: Comparison with previous work for representative designs

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Keccak-f[1600] in NANGATE 45nm ($m=0$)										
		AREA [kGE]						Rand.	f_{max}	Cycles
		Evaluation				Prep.	Total			
Order	**Design**	χ	θ	State	Σ			[bpc]	[MHz]	[/]
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	Parallel-3sh [BDN+13]	40.6	19.2	56.8	116.6	-	116.6	4	592	25
	Kit	0.5	0.6	26.1	29.1	0.7	29.8	50	1538	10776
	Serial-Area [GSM17]	0.4	0.4	14.5	15.7	-	15.7	-	850	3160
	Serial-3sh [BDN+13]	0.6	0.3	38.1	39.0	-	39.0	< 1	645	1625
2	Blaze	235.2	19.2	50.5	317.1	449.3	766.4	28800	884	25
	Parallel [GSM17]	114.0	22.5	51.1	188.1	-	188.1	4800	898	48
	Kit	0.7	1.0	39.1	43.7	1.4	45.1	90	1351	10776
	Serial-Area [GSM17]	2.2	0.6	21.4	24.2	-	24.2	75	898	3160
Keccak-f[200] in NANGATE 45nm ($m=0$)										
1	Blaze	18.1	1.6	4.2	25.2	28.9	54.0	2000	892	19
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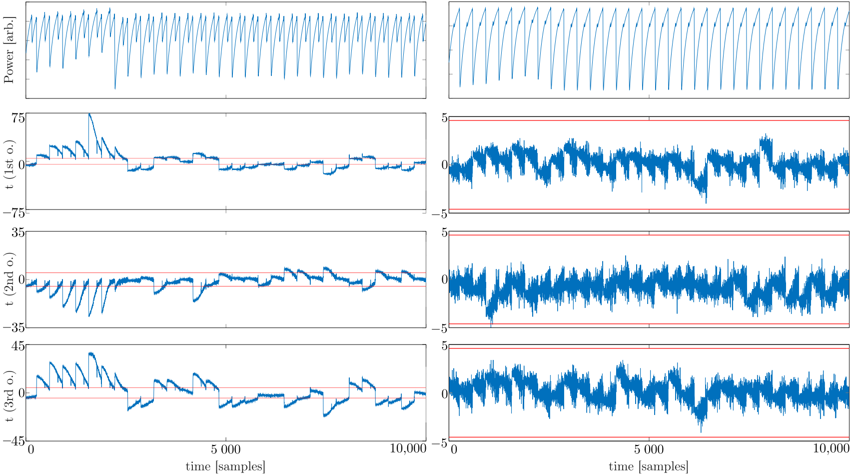
Leakage detection (Kit, $d = 3$, $m = 2$)



(a) Masks off (b) Masks on

Platform: Sakura-G board (2x Xilinx Spartan 6 FPGA)

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Leakage detection - over time

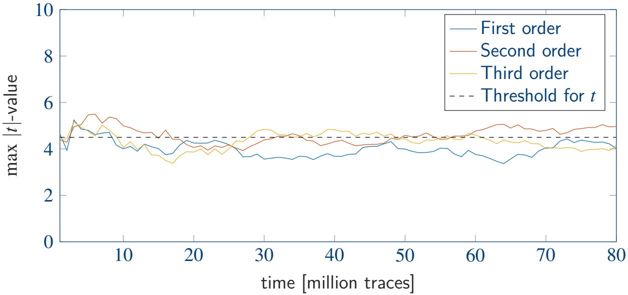

Figure: Maximum t-test value over time

Fault coverage (Kit, $d = 2$, m varies)

	$\boldsymbol{m} = 2$	$\boldsymbol{m} = 4$	$\boldsymbol{m} = 6$	$\boldsymbol{m} = 8$
# valid $\langle \boldsymbol{f} \rangle$	32	512	8192	131072
# detected $\langle \boldsymbol{f} \rangle$	24	480	8064	130560

Table: Experimental fault resistance results

- Simulation-based testing (HDL): fault vectors $\langle \boldsymbol{f} \rangle$
- Fault at different locations but stick to one MAC key guess
- Deterministic experiment: $1 - 2^{-m}$
- Extrapolate results for $m > 8$

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Conclusion and future work

- First implementations of KECCAK with resistance against combined attacks
  - Design space exploration: BLAZE, KIT and everything in between
  - Combined countermeasures skew the hardware design space
- Performance assessment as a function of the security parameters b, m, d [see paper]
- More efficient preprocessing stage, generally applicable [see paper]
- Currently only the small implementations have realistic requirements
  - Relax attacker model?
  - Define authentication tag in a different way?

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